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10/759,193	01/20/2004	Tsutomu Yamada	500.43408X00	7703

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EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,193	YAMADA ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-13 and 21* is/are pending in the application.

4a) Of the above claim(s) *4,9,12 and 13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-8,10,11 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *4,9,12 and 13* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
10/6/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4 – 13, and 21 are pending.

Election/Restrictions

2. Newly submitted claims 4, 9, and 12 – 13 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claim 4 is directed to a module computer system that moves module select signals to different terminals. This is independent and distinct from claims 1 and 21 because neither claims 1 or 21 recite moving select signals to different terminals. The amended material in claim 4 was not claimed in the originally presented claims. If the limitation had been presented as an independent claim originally, it would have been subject to a restriction / election requirement before the first office action.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 4, 9, and 12 – 13 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Response to Arguments

3. Applicant's arguments filed 08 august 2006 have been fully considered but they are not persuasive.

As per claims 1 and 21, Applicant argues that the relied upon references, US Patent No. 4,727,475 (hereinafter Kiremidjian) and US Patent 6,003,097 (hereinafter Richman), do not teach that the processing module selects from differing preset bus configuration parameters and device drivers, from a memory, for accessing differing types of I/O modules (See remarks; Page 10 and 11). However, the Examiner submits that Richman does teach this limitation. Richman teaches selecting differing bus configurations to access a specific bus (Richman; Col 6 Lines 51 – 64) and also teaches selecting device drivers to access I/O modules (Richman; Col 4 Line 66 – Col 5 Line 9).

As per claim 10, Applicant argues that the relied upon references do not teach that the ID generation part generates the identification information as a serial signal on the basis of the activate signal and a clock signal. However, serial and parallel data signals are well known in the art as a way to transmit information over a single wire or multiple wires. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a serial signal to transmit the identification information.

Claim Objections

4. Claims 1 and 21 are objected to because of the following informalities:

- Claim 1 – The claim recites "the identification information ***in association in accordance*** with and output order" (emphasis added) in line 22 of the claim. It appears that either "in association" or "in accordance" should be removed.
- Claim 21 – The claim recites "the identification information ***in association in accordance*** with and output order" (emphasis added) in line 27 of the claim. It appears that either "in association" or "in accordance" should be removed.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the module" in Line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the "processing module" or the "plurality of I/O modules" of the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,727,475 (hereinafter Kiremidjian) in view of US Patent 6,003,097 (hereinafter Richman).

As per claim 1, Kiremidjian teaches a modular computer system (Kiremidjian; Figure 1, Col 4 Lines 26 – 27) formed by connecting a processing module (Kiremidjian; Figure 1 Item 15, Col 4 Lines 32 – 35) having a processor mounted thereon and a plurality of I/O modules (Kiremidjian; Figure 1 Items 16 – 18, Col 4 Lines 39 – 42) in a stacked form via connectors forming a bus (Kiremidjian; Figure 1 Item 11, Col 4 Lines 45 – 49), wherein each I/O module comprises a module exclusive selection part (Kiremidjian; Col 6 Lines 45 – 52) for activating the module responsive to a module select signal input from a terminal in a predetermined position on a processing module side connector (Kiremidjian; Col 3 Lines 1 – 6), the predetermined position being the same for the I/O modules (Kiremidjian; Col 3 Lines 1 – 12); and an ID output part for outputting identification information of its own I/O module (Kiremidjian; Figure 4 Item 21, Col 5 Lines 5 – 18) to a predetermined terminal on the connector (Kiremidjian; Col 3 Lines 1 – 12) on the basis of the module select signal output from said module exclusive selection part (Kiremidjian; Col 6 Lines 45 – 52); wherein the processing module

comprises a module select signal output part for outputting the module select signal to a connector terminal to which the I/O module is connected (Kiremidjian; Col 6 Lines 42 – 45); and an ID input part for taking in the identification information output to the predetermined terminal on the connector (Kiremidjian; Col 6 Lines 52 – 55), said module select signal output part outputs the module select signal successively to the I/O modules connected to the processing modules (Kiremidjian; Col 7 Lines 9 – 19), and said ID input part recognized the I/O modules and the identification information in accordance with an output order of the module select signal (Kiremidjian; Col 7 Lines 19 – 26).

Kiremidjian does not teach wherein in accordance with the association of the I/O modules with identification information, the processing module selects from differing preset bus configuration parameters and device drivers, from a memory, for accessing differing types of the I/O modules.

However, Richman teaches wherein in accordance with the association of the I/O modules with identification information, the processing module selects from differing preset bus configuration parameters (Richman; Col 6 Lines 49 – 64) and device drivers (Richman; Col 4 Line 66 – Col 5 Line 9), from a memory, for accessing differing types of the I/O modules.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Kiremidjian to include the bus configuration parameters and device drivers because doing so allows for the

operating system of the computer to be independent of the characteristics of a computer bus architecture (Richman; Col 6 Lines 61 – 64).

As per claim 5, Kiremidjian also teaches wherein said module exclusive selection part has a plurality of wires connected to a plurality of connector terminals of the input connector on the processing module side (Kiremidjian; Figure 4, Col 6 Lines 37 – 55), one of the wires is connected to said ID output part (Kiremidjian; Figure 4 Item "XIORD"), and one of other wires is connected to a terminal that is included in a plurality of connector terminals on the output connector, and that is in the same position as that of the connector terminal supplies with a module select signal that selects its own module (Kiremidjian; Figure 4, Col 5 Lines 39 – 66).

As per claim 6, Kiremidjian also teaches wherein said module exclusive selection part is formed by connecting a D terminal of a D type flip-flop to one of connector terminals on the input connector (Kiremidjian; Figure 4 Item "XPIN+", Col 5 Lines 39 - 66), connecting a Q output terminal of said D type flip-flop to said ID output part (Kiremidjian; Figure 4 [a Q- output coupled as one input to NAND gate 32], Col 5 Lines 39 – 66) and to a terminal that is included in the output connector and that is in the same position as that of the connector terminal to which the D terminal is connected, and connecting a clock terminal of said D type flip-flop to a terminal to which connector terminals on the input connector and output connector are connected in common

(Kiremidjian; Figure 4 Item "XIOWR" [control signal supplied to the polling logic in each module], Column 5 Lines 19 – 66).

As per claim 7, Kiremidjian also teaches wherein said processing module drives the connector terminal to which the clock terminal is connector terminal to which the D terminal is connected, with an enable signal (Kiremidjian; Figure 4 Item "XIOWR" [control signal supplied to the polling logic in each module], Col 6 Line 37 – Col 7 Line 14).

As per claim 8, Kiremidjian also teaches wherein said ID output part comprises an ID generation part (Kiremidjian; Figure 4 Item 21) for generating identification information of its own module (Kiremidjian; Col 5 Lines 5 – 18); and an output enable part (Kiremidjian; Figure 4 Item 32 "ID ENABLE", Col 6 Lines 37 – 55) for outputting the identification information generated by said ID generation part to a predetermined terminal on the input connector (Kiremidjian; Col 5 Lines 5 – 18).

As per claim 10, Kiremidjian in combination with Richman also obviously teaches wherein said ID generation part generates the identification information as a serial signal on the basis of the activate signal and a clock signal because serial signals are well known in the art as a technique used to transmit data.

As per claim 11, Kiremidjian also teaches wherein said ID output part is formed by connecting wires driven by the activate signal to a plurality of predetermined terminals on the connector via PN-junction elements according to the identification information (Kiremidjian; Col 5 Lines 5 – 18).

As per claim 21, Kiremidjian teaches a modular computer system (Kiremidjian; Figure 1, Col 4 Lines 26 – 27) formed by connecting a processing module (Kiremidjian; Figure 1 Item 15, Col 4 Lines 32 – 35) having a processor mounted thereon and a plurality of I/O modules (Kiremidjian; Figure 1 Items 16 – 18, Col 4 Lines 39 – 42) in a stacked form via connectors forming a bus (Kiremidjian; Figure 1 Item 11, Col 4 Lines 45 – 49), wherein each I/O module comprises a module exclusive selection part for determining whether a module select signal input from a processing module side input connector is a signal that selects its own module (Kiremidjian; Col 6 Lines 45 – 52), and transmitting the module select signal to a terminal that is included in terminals on an output connector side opposite to the processing module and that is in the same position as that of a terminal on the input connector supplied with the signal that selects its own module (Kiremidjian; Col 5 Lines 64 – 66), when the module select signal input from the input connector is a signal that selects another module (Kiremidjian; Col 7 Lines 9 – 14); and an ID output part for outputting identification information of its own I/O module (Kiremidjian; Figure 4 Item 21, Col 5 Lines 5 – 18) to a predetermined terminal on the connector (Kiremidjian; Col 3 Lines 1 – 12); wherein the processing module comprises a module select signal output part for outputting the module select

signal to a connector terminal to which a first I/O module is connected (Kiremidjian; Col 6 Lines 42 – 45); and an ID input part for taking in the identification information output to the predetermined terminal on the connector (Kiremidjian; Col 6 Lines 52 – 55), said module select signal output part outputs the module select signal successively to the I/O modules connected to the processing modules (Kiremidjian; Col 7 Lines 9 – 19), and said ID input part recognized the I/O modules and the identification information in accordance with an output order of the module select signal (Kiremidjian; Col 7 Lines 19 – 26).

Kiremidjian does not teach wherein in accordance with the association of the I/O modules with identification information, the processing module selects from differing preset bus configuration parameters and device drivers, from a memory, for accessing differing types of the I/O modules.

However, Richman teaches wherein in accordance with the association of the I/O modules with identification information, the processing module selects from differing preset bus configuration parameters (Richman; Col 6 Lines 49 – 64) and device drivers (Richman; Col 4 Line 66 – Col 5 Line 9), from a memory, for accessing differing types of the I/O modules.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Kiremidjian to include the bus configuration parameters and device drivers because doing so allows for the operating system of the computer to be independent of the characteristics of a computer bus architecture (Richman; Col 6 Lines 61 – 64).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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